Multilayered Power Supply Line for Semiconductor Integrated Circuit and Layout Method thereof

Background of the Invention

Field of the Invention:

The present invention relates to a multilayered power supply line of an MTM (Metal-Insulator-Metal) structure, which supplies power to an I/O (Input/Output) buffer and an internal circuit in a semiconductor integrated circuit, and a method of laying out the multilayered power supply line.

This application is counterpart of Japanese patent application, Serial Number 397724/2003, filed November 27, 2003, the subject matter of which is incorporated herein by reference.

Description of the Related Art:

As general multilayered power supply lines each suitable for use in a semiconductor integrated circuit, which supply power to I/O buffers and internal circuits, there have heretofore been known one laid out with a wiring metal of one layer being provided in such a power supply line as shown in Fig. 9, and one laid out using a multilayered wiring metal such that the impedance of a power supply line becomes low. A sectional view of the power supply line shown in Fig. 9, which is taken along a dotted line 98, is shown in Fig. 10.

As such a multilayered wiring metal, there has been

known a power supply line described in the following Patent Document 1, for example. In the present power supply line, a first metal layer is added to an area free of an I/O buffer of a chip corner unit, and parallel plate condensers are respectively formed between the first metal layer, and a VDD power supply line and a GND power supply line to increase capacity, thereby making it possible to reduce noise caused by switching of the I/O buffer.

Since a first power supply wiring layer supplied with a power supply or source potential from an external power supply, and a second power supply wiring layer supplied with a ground potential are formed in multilayer form in a semiconductor device described in the following Patent Document 2, the wiring resistances of the first and second power supply wiring layers can be reduced. Therefore, a power supply or source potential low in impedance and a ground potential can be supplied to each circuit block in an internal circuit.

Patent Document 1

Japanese Laid-Open patent No. 1997-246476.

Patent Document 2

Japanese Laid-Open patent No. 2000-311964

Methods such as expanding of a wiring width, multilayering of wirings as in the case of the above-described Patent Documents 1 and 2 or the like have been used in the multilayered power supply lines employed in

the semiconductor integrated circuits in order to reduce impedance.

However, a chip area increases with the expansion of the wiring width, and wiring's multilayering encounters difficulties in wiring other signal lines. Since the VDD and GND power supply lines are relatively small in capacity, switching noise is apt to occur in the semiconductor integrated circuit.

Summary of the Invention

The present invention has been made to solve the drawbacks of such prior arts and aims to provide a multilayered power supply line which supplies power to an I/O buffer and an internal circuit at low impedance without expanding the width of each of power supply lines and multilayering them and without making it difficult to wire other signal lines, and a layout method thereof.

According to one aspect of the present invention, there is provided a multilayered power supply line of an MIM (Metal-Insulator-Metal) structure, comprising:

a first metal layer which serves as a wiring metal;

a second metal layer located below the first metal layer; and

a third metal layer serving as a capacitor metal, which is located between the first metal layer and the second metal layer,

wherein an insulator is embedded into gap portions

defined among these metal layers,

the second metal layer is electrically connected to the first metal layer and thereby supplied with power identical in potential to the first metal layer, and

the third metal layer is electrically connected to the first metal layer and thereby supplied with the power identical in potential to the first metal layer.

According to another aspect of the present invention (this aspect is referred to as aspect 1), there is provided a method of laying out a multilayered power supply line having an MIM structure wherein a first metal layer that serves as a wiring metal is disposed over a second metal layer, a third metal layer that serves as a capacitor metal is disposed between the first metal layer and the second metal layer, and an insulator is embedded into gap portions defined among these metal layers, the method comprising the following steps of:

electrically connecting the second metal layer to the first metal layer to allow the first metal layer and the second metal layer to be identical in potential to each other; and

electrically connecting the third metal layer to the first metal layer to allow the first metal layer and the third metal layer to be identical in potential to each other.

Furthermore, following various aspects are disclosed in the specification. These aspects are as

follows.

A method according to the aspect 1, further comprises the step of: causing the second metal layer and the third metal layer to be identical in potential to each other and thereby using the third metal layer as a wiring metal. (Aspect 2)

A method according to aspect 2, further comprising the step of:

supplying a source potential of an external power supply to the first metal layer and supplying the source potential of the external power supply even to the second metal layer and the third metal layer. (Aspect 3)

A method according to aspect 2, further comprising the step of:

supplying a ground potential to the first metal layer and supplying the ground potential even to the second metal layer and the third metal layer. (Aspect 4)

A method according to aspect 1, further comprising the steps of:

alternately disposing, as the first metal layer, metal layers supplied with the source potential of the external power supply and metal layers supplied with the ground potential, and

constituting capacitors in potential different positions between the first metal layer and the second metal layer and between the first metal layer and the third metal layer. (Aspect 5)

A method according to aspect 5, further comprising the steps of:

constituting a first 3-layer multilayered power supply line by a second metal layer supplied with the ground potential and a third metal layer supplied with the source potential of the external power supply, and

constituting a second 3-layer multilayered power supply line by a second metal layer supplied with the source potential of the external power supply and a third metal layer supplied with the ground potential. (Aspect 5)

A method according to aspect 5, further comprising the step of constituting, in the first metal layer, a capacitor using a parasitic capacitance developed between a metal layer supplied with the source potential of the external power supply and a metal layer supplied with the ground potential. (Aspect 6)

A method of laying out a multilayered power supply line including a capacitor metal, comprising the following steps of:

using the capacitor metal as a wiring metal with being substituted therewith; and

increasing the wiring metal by one layer on a pseudo basis. (Aspect 7)

According to the multilayered power supply line of the present invention, a metal, which is originally used as a capacitor metal, is used as a wiring metal in a

wiring metal 3-layer multilayered power supply line of an MIM structure so as to become identical in potential to a top metal and a second metal, thereby making it possible to reduce the impedance of the power supply line. At this time, the multilayered power supply line of the present invention does not interfere with wiring of other signal lines.

According to the present invention as well, in a multilayered power supply line, parallel-running VDD power supply lines and GND power supply lines are alternately superposed on one another, and a normal capacitor made up of a capacitor metal and a second metal and a second capacitor made up of a top metal and a capacitor metal are used, so that switching noise can be reduced with the capacitors each having large capacity. Each capacitor metal is caused to function as a source or power supply line, thereby making it possible to obtain a low impedance multilayered power supply line while being held in a chip area identical in size to the conventional one.

Brief Description of the Drawings

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter which is regarded as the invention, it is believed that the invention, the objects and features of the invention and further objects, features and

advantages thereof will be better understood from the following description taken in connection with the accompanying drawings in which:

Fig. 1 is a diagram showing one embodiment of a multilayered power supply line according to the present invention;

Fig. 2 is a diagram illustrating, in sectional form, the multilayered power supply line shown in Fig. 1;

Fig. 3 is a schematic diagram depicting the multilayered power supply line shown in Fig. 1 applied to a block cell;

Fig. 4 is a schematic diagram showing the multilayered power supply line shown in Fig. 1 applied to a block cell;

Fig. 5 is a schematic diagram illustrating the multilayered power supply line shown in Fig. 1 applied to a block cell;

Fig. 6 is a schematic diagram depicting the multilayered power supply line shown in Fig. 1 applied to a block cell;

Fig. 7 is a diagram showing a signal line wired to the multilayered power supply line shown in Fig. 1;

Fig. 8 is a diagram illustrating, in sectional form, the multilayered power supply line shown in Fig. 7 and the signal line;

Fig. 9 is a diagram depicting a conventional multilayered power supply line;

Fig. 10 is a diagram showing, in sectional form, the conventional multilayered power supply line shown in Fig. 9;

Fig. 11 is a diagram illustrating another embodiment of a multilayered power supply line according to the present invention;

Fig. 12 is a diagram showing, in sectional form, the multilayered power supply line shown in Fig. 11; and

Fig. 13 is a diagram illustrating a further embodiment of a multilayered power supply line according to the present invention.

Detailed Description of the Invention

Preferred embodiments of the present invention will hereinafter be described in detail with reference to the accompanying drawings.

One embodiment of a multilayered power supply line employed in a semiconductor integrated circuit, according to the present invention will next be explained in detail with reference to the accompanying drawings. The multilayered power supply line 10 according to the present embodiment can be applied to both a VDD power supply line for supplying a power supply or source potential and a GND power supply line for supplying a ground potential. The VDD power supply line and the GND power supply line to which the multilayered power supply line 10 is applied, may be wired so as to surround the

periphery of a block cell 30 as shown in Fig. 3, for example or may be wired as shown in Fig. 4, 5 or 6. Part of the VDD power supply line shown in Fig. 3 is shown in an enlarged form, and a sectional view of the VDD power supply line shown in Fig. 1, which is taken along a dotted line 50, is shown in Fig. 2.

Referring to Figs. 1 and 2, the embodiment of the multilayered power supply line 10 employed in the semiconductor integrated circuit, according to the present invention is configured in such a manner that a top metal 12 and a second metal 14 are electrically connected to each other by through holes 18, and a capacitor metal 16 is electrically connected to the top metal 12 by through holes 20. The embodiment of the multilayered power supply line 10 supplies power to an I/O buffer and an internal circuit employed in the semiconductor integrated circuit. Incidentally, a diagrammatic illustration of portions directly irrelevant to the understanding of the present invention is omitted and redundant descriptions will therefore be avoided.

In the present embodiment, conductive materials such as aluminum, copper, cobalt, etc. may be used for the top metal 12, the second metal 14, the capacitor metal 16, the through holes 18 and the through holes 20. In the multilayered power supply line 10, an insulator such as silicon oxide (SiO_2) is embedded into gap or clearance portions defined among these materials.

In a manner similar to a metal 3-layer MIM capacitor process or the like, the multilayered power supply line 10 according to the present embodiment is made up of three layers: the top metal 12, the second metal 14 corresponding to a bottom plate, and the capacitor metal 16 corresponding to a top plate. Since, however, the second metal 14 is electrically connected to the top metal 12 via the through holes 18 in the present invention, the second metal 14 becomes identical in potential to the top metal 12. Particularly since the capacitor metal 16 is used as a wiring metal and electrically connected to the top metal 12 via the through holes 20, the capacitor metal 16 becomes identical in potential to the top metal 12.

The multilayered power supply line 10 can be applied to both the VDD power supply line and the GND power supply line. For instance, when the top metal 12 is of a VDD power supply level, the second metal 14 and the capacitor metal 16 result in the VDD power supply level. When the top metal 12 is a GND power supply level, the second metal 14 and the capacitor metal 16 result in the GND power supply level.

Thus, the top metal 12, the second metal 14 and the capacitor metal 16 become identical to one another in potential. The multilayered power supply line 10 according to the present embodiment does not function as a capacitor but as a multilayered power supply line using

a normal wiring metal, e.g., a low-impedance multilayered power supply line as in a wiring metal 3-layer multilayered power supply line or the like.

Since the multilayered power supply line 10 results in three layers without being formed as two layers when the top metal 12, the second metal 14 and the capacitor metal 16 employed in the multilayered power supply line 10 are respectively identical in wiring width, the source impedance simply results in 2/3. This means that assuming that current consumption of a headphone amplifier is 20mA in the case of a low impedance drive circuit (e.g., 16-Ω load drive in the case of the headphone amplifier), only a difference in 1 Ω occurs in the source impedance and a voltage drop in the power supply normally results in 20mV. In the multilayered power supply line according to the present embodiment at this time, the voltage drop results in 13mV of 2/3, so that a larger effect is obtained. When the multilayered power supply line according to the present embodiment is used in a digital circuit, the width of each power supply line can be reduced while the impedance is being maintained as it is, thus making it possible to bring about the expectation of high integration.

Applying a method of laying out the multilayered power supply line as described in the present invention makes it possible to increase the wiring metal by one layer on a pseudo or dummy basis owing to the substituted

use of the capacitor metal as the wiring metal in the metal 3-layer MIM capacitor process or the like containing the capacitor metal, for example. At this time, the multilayered power supply line 10 according to the present embodiment is capable of maintaining the 3-layer multilayered power supply line without increasing a chip area and impedance of each power supply line and interfering with wiring of a signal line 70 or the like as shown in Fig. 7. A sectional view of the multilayered power supply line shown in Fig. 7, which is taken along a dotted line 80, is illustrated in Fig. 8. Since the capacitor metal 16 is located between the top metal 12 and the second metal 14 in the present embodiment, there is little effect of affecting the signal line 70 by the multilayered power supply line 10. Thus, the substitution of the capacitor metal with the wiring metal can be applied not only to the 3-layer multilayered power supply line but also to a multilayered power supply line of four or more layers.

As another embodiment, as shown in Fig. 11, a multilayered power supply line 100 is configured in such a manner that a plurality of VDD power supply lines and GND power supply lines run parallel to one another and 3-layer multilayered power supply lines 130 and 140 having VDD power supply lines and GND power supply lines run parallel to each other. The 3-layer multilayered power supply lines 130 and 140 may respectively be configured

as in the case of, for example, a metal 3-layer MIM capacitor process.

In the multilayered power supply line 100 according to the present embodiment, as shown in Fig. 11, top metals 102, 104, 106 and 108 are provided so as to cross over the 3-layer multilayered power supply lines 130 and 140. Top, capacitor and second metals are made up of VDD and GND power lines arranged alternately. At this time, the top metals 102 and 104 are electrically connected to the corresponding second metal 142 in the 3-layer multilayered power supply line 140 and the corresponding capacitor metal 134 in the 3-layer multilayered power supply line 130 via through holes 120. The top metals 106 and 108 are electrically connected to the corresponding second metal 132 in the 3-layer multilayered power supply line 130 and the corresponding capacitor metal 144 in the 3-layer multilayered power supply line 140 via through holes 122.

In the present embodiment, the top metals 102 and 104 are supplied with a power supply or source potential by being connected to an unillustrated external power supply or the like and function as VDD power supply lines. On the other hand, the top metals 106 and 108 are grounded and thereby supplied with a ground potential although not shown in the drawing and function as GND power supply lines.

Thus, since the second metal 144 and the capacitor

metal 134 are respectively connected to the top metals 102 and 104 corresponding to the VDD power supply lines, they are supplied with the power supply potential and function as the VDD power supply lines. Since the second metal 132 and the capacitor metal 144 are connected to their corresponding top metals 106 and 108 corresponding to the GND power supply lines, they are supplied with the ground potential and function as the GND power supply lines.

Now, a sectional view of the multilayered power supply line shown in Fig. 11, which is taken along a dotted line 150, is illustrated in Fig. 12. As a result, the 3-layer multilayered power supply line 130 in which the top metal 108 and the second metal 132 are connected via the through holes 122, and the 3-layer multilayered power supply line 140 in which the top metal 102 and the second metal 142 are connected via the through holes 120, are shown in the figure.

At this time, in the 3-layer multilayered power supply line 130, the capacitor metal 134 corresponding to the VDD power supply line is wired between the top metal 108 and the second metal 132 both corresponding to the GND power supply lines. Therefore, a difference in potential occurs between the top metal 108 and the capacitor metal 134 so that the capacitor metal 134 functions as a parallel plate condenser 162. A difference in potential occurs between the second metal 132 and the

capacitor metal 134 so that the capacitor metal 134 functions as a parallel plate condenser 164.

On the other hand, in the 3-layer multilayered power supply line 140, the capacitor metal 144 is wired between the top metal 102 and the second metal 142 both corresponding to the VDD power supply lines. Therefore, a difference in potential occurs between the top metal 102 and the capacitor metal 144 so that the capacitor metal 144 functions as a parallel plate condenser 172. A difference in potential occurs between the second metal 142 and the capacitor metal 144 so that the capacitor metal 144 functions as a parallel plate condenser 174.

These parallel plate condensers 162, 164, 172 and 174 allow the capacitor metals 134 and 144 to function as the VDD and GND power supply lines respectively.

Thus, the multilayered power supply line 100 according to the present embodiment is provided with the parallel-running VDD power supply lines and GND power supply lines alternately superposed on one another and includes the second capacitor comprised of the top metal and the capacitor metal in addition to the normal capacitor made up of the capacitor metal and the second metal. Thus, the multilayered power supply line 100 has the capacitor having capacity larger than one where it has the normal capacitor alone, so that switching noise can be reduced. Further, the capacitor metal is caused to function as the power supply line, so that a low

impedance power supply line can be obtained while it is being held in a chip area identical in size to the conventional one.

In the present embodiment, the top metal is low in impedance because it is thicker than other metals, and is advantageously used in both the VDD and GND power supply lines.

Applying the multilayered power supply line according to the present embodiment to a ring of an I/O buffer makes it possible to reduce source impedance and switching noise developed due to an increase in capacitance between a VDD power supply and a GND power supply without increasing the chip area and changing a process.

The multilayered power supply line 100 according to the present embodiment has been configured in such a manner that the parallel-running VDD power supply lines and GND power supply lines overlap alternately. However, as in a multilayered power supply line 180 shown in Fig. 13, metals each corresponding to a VDD power supply line and metals each corresponding to a GND power supply line are alternately laid out in top metals 182. Thereafter, a second metal 184 and a capacitor metal 184 may be electrically connected to these metals. At this time, a difference in potential occurs between the adjacent top metals 182 so that parasitic capacity increases. Further, the parasitic capacity is set as a bypass condenser in

addition to a capacitor between the top metal 182 and the second metal 184 and a capacitor between the top metal 182 and the capacitor metal 186, thereby making it possible to reduce switching noise.

While the present invention has been described with reference to the illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to those skilled in the art on reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.